Amendments to the Claims:

The following listing of claims will replace all prior versions, and listings, of claims in the application:

1.-78. (Canceled)

79. (Currently Amended) An active matrix substrate, comprising:

a plurality of scan lines;

a plurality of data lines;

a plurality of pixel transistors corresponding to intersections of the plurality of scan lines and the plurality of data lines;

a first data line driving circuit connected to a first end of each of the plurality of data lines; and

at least one analog video signal line providing an analog video signal to the first data driving circuit,

the first data line driving circuit including a shift ~~resistor~~ register and a gate circuit, the gate circuit including at least a NAND gate, the NAND gate inputting an output signal from the shift ~~resistor~~ register and an enable signal.

80. (Currently Amended) An active matrix substrate, comprising:

a plurality of scan lines;

a plurality of data lines;

a plurality of pixel transistors corresponding to intersections of the plurality of scan lines and the plurality of data lines;

a first data line driving circuit connected to a first end of each of the plurality of data lines; and

at least one analog video signal line providing an analog video signal to the first data line driving circuit,

the first data line driving circuit including a shift ~~resistor~~ register and a gate circuit, the gate circuit including ~~at least a~~ a plurality of XOR ~~gate~~gates, each of the XOR ~~gate~~ gates inputting ~~at least~~only two output signals, the two output signals being outputted from the shift ~~resistor.~~register.

81-83. (Canceled)

84. (New) A driving circuit comprising:

a shift register;

a first output enable signal line;

a second output enable signal line;

a video signal line;

a plurality of first NAND circuits, each of the first NAND circuits electrically connecting the shift register, the each of the first NAND circuits electrically connecting the first output enable signal line;

a plurality of second NAND circuits, each of the second NAND circuits electrically connecting the shift register, the each of the second NAND circuits electrically connecting the second output enable signal line; and

a plurality of analog switches electrically connecting the video signal line and each of the plurality of analog switches electrically connecting one of the first NAND circuits and the second NAND circuits.

85. (New) The driving circuit according to claim 84, the first NAND circuits and the second NAND circuits being arranged alternately.

86. (New) An active matrix substrate comprising:

a plurality of scan lines;

a plurality of data lines crossing the scan lines, the active matrix substrate; and

the driving circuit according to claim 84, the plurality of analog switches electrically connecting the plurality of the data lines.

87. (New) The active matrix substrate according to claim 86, the first output enable signal line outputting a first output enable signal, the second output enable signal line outputting a second output enable signal, the second output enable signal line being at a high level when the first output enable signal is at a low level during a pulse generation period, and the second output enable signal being at a low level when the first output enable signal is at a high level in the pulse generation period.

88. (New) The active matrix substrate according to claim 86, the shift register having multiple stages, each of the multiple stages of the shift register being responsive to one of a first clock signal and a second clock signal.

89. (New) The active matrix substrate according to claim 88, the first clock signal being at a high level when the first output enable signal is at a high level, and the first clock signal being at a low level when the first output enable signal is at a low level in a pulse generation period.

90. (New) A display device, comprising:

a plurality of scan lines;

a plurality of data lines crossing the scan lines, the active matrix substrate; and

the driving circuit according to claim 84, the plurality of analog switches electrically connecting the plurality of the data lines.

91. (New) A driving circuit, comprising:

a shift register;

a plurality of XOR gates, each of the XOR gates electrically connecting the shift register, the each of the XOR gates receiving two outputs from the shift register;

a video signal line; and

a plurality of analog switches, each of the analog switches electrically connecting the XOR gates and the video signal line.

92. (New) An active matrix substrate comprising:

a plurality of scan lines;

a plurality of data lines crossing the scan lines; and

the driving circuit according to claim 90, the plurality of analog switches electrically connecting the plurality of the data lines.

93. (New) A display device comprising:

a plurality of scan lines;

a plurality of data lines crossing the scan lines; and

the driving circuit according to claim 90, the plurality of analog switches electrically connecting the plurality of the data lines.